Analytical Results for the I-V Characteristics of a Fully Depleted SOI-MOSFET

H. Morris, E. Cumberbatch, V. Tyree, H. Abebe

Abstract: Explicit formulae for the I-V characteristics of an SOI/SOS MOSFET operating in the fully depleted mode are derived by extending the asymptotic method of Ward. A detailed comparison with test data is presented and the model is shown to be effective over a range of device geometries for a half micrometer technology and voltages up to and including the kink attributable to impact ionization.

1 Introduction

Silicon-on-insulator (SOI) technology has been of interest since the 1970's due to advantages in device isolation and speed, etc., over regular MOSFET's, [1], [2]. A common difficulty with SOI technologies has been obtaining accurate SPICE simulations of circuits that correctly model SOI device behavior, including the "kink" effect.

SPICE software requires current-voltage (I-V) formulae for the transistor elements in circuits, and modeling the I-V relationships for SOI devices has introduced only small variations from the standard bulk MOSFET formulae, [3]-[5]. The latter, at small channel lengths, now require up to 200 parameters in their descriptions. This formulation requires extensive test data and identification, an expensive and time-consuming operation.

Among the efforts to reduce over-parametrization and return to a fundamental, physics-based description, we have been developing the asymptotic analysis developed by Ward [6] [7].This work approached the partial differential equations governing the flow of electrons and holes [8][9], in terms of

1. A perturbation expansion based on the small parameter measuring the ratio of depletion layer depth to channel length. The first term in this expansion gives the ``quasi-one-dimensional approximation,'' which is the standard approximation usually adopted, based on ``long channel'' arguments. Ward shows how to improve on this approximation to include source and drain corner effects, but the analysis is limited to small drain voltages.

2. An asymptotic solution to the quasi-1-D equations based on the large parameter measuring the ratio of doping to the intrinsic level.

This approach identifies the electron-rich inversion region as a thin boundary layer, and applies the method of matched asymptotic expansions [10]. This approach was introduced in semi-conductor physics by Please, [11] for the p-n junction, and Ward extended it to the MOSFET device. The Ward asymptotic solution requires numerical work (to solve transcendental equations) and the I-V formulae require an integral to be computed numerically. Recently, [12] we carried forward that work, making further approximations to achieve I-V formulae that are accurate over a wide range of device sizes and voltages and

H. Abebe (e-mail: abebeh@mosis.org) and V. Tyree (e-mail: tyree@mosis.org) are with MOSIS, Information Sciences Institute, University of Southern California, 4676 Admiralty Way, Marina Del Rey, CA 90292, USA. Tel: (310) 448-8740 Fax: (310) 823-5624
H. Morris is with Department of Mathematics, San Jose State University, San Jose, CA 95192, USA (e-mail: morris@math.sjsu.edu).
E. Cumberbatch is with Depertment of Mathematics, Claremont Graduate School, Claremont, CA 91711, USA (e-mail: ellis.cumberbatch@cgu.edu).

require only a simple iteration to obtain results. This work has been further extended to the SOI device, and, in the case in which the silicon is fully depleted, *explicit* I-V formulae have been obtained that are accurate when compared with data. These formulae involve parameters that have been identified from data. They give substantial simplifications over standard I-V formulae, and provide an important evolution in device modeling. A multi dimensional analysis of the semiconductor equations is mostly useful to the device simulation level. For a circuit modeling point of view, usually 1-D solutions are enough to reveal the critical information need even for a nano scale devices. In circuit analysis, compact 1-D analytical solutions are preferable because of their simplicity, computational speed, and suitability for practical SPICE application, [15].

2 Equations and Solution

For reference purposes we give the equations on which the solutions are based. In terms of scaled variables, which are defined in the Tables 1 and 2, the quasi-1-D charge equation is:

$$\frac{\partial^2 w}{\partial x^2} = e^{(w-1-\varphi)\ln(\lambda)} - e^{-(w+1)\ln(\lambda)} + 1 \tag{2.1}$$

where x is co-ordinate perpendicular to the channel, $\varphi = \varphi(y)$ is the scaled quasi-Fermi potential, and y is the co-ordinate along the channel. The parameter λ the ratio of silicon doping to the intrinsic level is of the order $10^6 - 10^7$. The matched asymptotic expansions technique assesses the size of each term in (2.1) in various regimes: inversion layer, depletion layer, bulk. Several of the terms may be omitted in each layer, allowing solutions to be generated for the terms remaining. The integration constants that occur must then be related by matching the solutions across overlapping boundaries in a non-trivial way. The solution for the SOI device in the fully depleted mode has a substantial simplification over the standard MOSFET: the interface at the silicon/insulator base is a known boundary (the boundary condition of zero normal field is applied there) and is not an unknown free boundary as it is for the standard MOSFET. The solution in the silicon provides a relationship between the quasi-Fermi potential and the electric potential and field at the silicon/gate insulator interface. At that interface there is also the continuity of electric displacement, providing a relationship between the applied gate voltage and the electric potential end field. Utilizing these two relationships to eliminate the field is rarely possible without numerical help, but in this case we were able to find an accurate approximation (equation (2.4)).

We refer to [12], for details of this analysis and for computation of the current, which follows standard routines. The integrals for the current can be performed explicitly. Results of this work are:

2.1 Linear Region

$$I_{ds} = \mu I_c \sqrt{2\lambda b^3} [-c\sqrt{\frac{b}{8}}(V_{gs}{}^* - w_s) + (c\sqrt{\frac{2}{b}} - \frac{d}{\sqrt{2}})w_s + \frac{\sqrt{2}d}{b}\ln(V_{gs}{}^* - w_s + \frac{d}{c\sqrt{b}})]_{w_{s0}}^{w_{s1}}$$

(2.2)

with $b = \ln(\lambda)$ and where w_{s0} and w_{s1} are the source and drain values of w_s (the scaled potential at $x = 0$). That is

$$w_{s0} = w_s(\varphi = 0), w_{s1} = w_s(\varphi = V_{ds}/b)$$

(2.3)

The constants I_c, c, d are determined by the model. The relationship of w_s with the gate voltage and quasi-Fermi potential is

given by

$$w_s = 1 + \varphi + \kappa[\frac{\ln(b)}{b} + \frac{1}{b}\ln(\frac{c^2 bV^2 - d^2}{2})], \kappa = \frac{c^2 bV^2 - d^2}{c^2 bV^2 - d^2 + 2c^2 V}$$

(2.4)

with $V = V_{gs}{}^* - 1 - \varphi$.

2.2 Saturation Region

The current has a contribution from the inverted region plus one from the depleted region:

$$I_{ds} = I_{ds,inverted} + I_{ds,depleted}$$

The first term is given by (2.2) with w_{s1} replaced by w_{sp0}, where

$$w_{sp0} = 1 + \varphi_{p0}, \varphi_{p0} = V_{gs}{}^* - 1 - \frac{d}{c\sqrt{b}}$$

(2.5)

The second term is given by

$$I_{ds,depleted} = \frac{\mu I_c}{d\sqrt{b\lambda}} e^{w_{sp0}b}(e^{-\varphi_{p0}b} - e^{-\bar{V}_{ds}})(1 + \frac{1}{d^2 b})$$

(2.6)

The model is completed by the choice of an electron mobility model. We have used the standard rational form

$$\mu = \frac{\mu_0}{1 + U_1(V_{gs} - V_T) + U_2(V_{gs} - V_T)^2}$$

(2.7)

where V_T is the threshold voltage. The threshold voltage is very useful for circuit designers, and it gives designers the value of

the gate voltage at which the transistor will be turned on. When the gate voltage reaches the threshold voltage, the substrate

underneath the gate becomes inverted. If the gate voltage is less than the threshold voltage, there is some leakage current in the

channel and the device operates in the so called sub-threshold regime.

3 Impact Ionization

The semi-conductor equations that we have used to derive our approximate formulae have explicitly excluded the physical phenomena that lead to the kink effect. To account for the rise in the drain-source current we introduce a simple conceptual model to justify a phenomenological correction term. If we attribute the kink effect entirely to impact ionization effects then we can write $I_{ds} = I_{ds0} + I_{kink}$ with $I_{kink} = M I_{ds0}$ where I_{ds0} is the current that would be obtained if impact ionization effects were absent. When impact ionization is present it provides a source of current and the electron current equation has the modified form

$$\nabla . J_n = G_{I-I}$$

where the impact ionization source is usually modeled by $G_{I-I} = -\alpha_n J_n$ with $\alpha_n = A_n \exp(-\beta_n / F)$ with α_n strongly dependent on the electric field strength F [13]. Adopting the assumptions of Jacunski *et al.* [14], but introducing a more accurate approximation, leads to the fitting function given by

$$M = \begin{cases} C_1 \mathrm{expint}(C_2 /(V_{ds} - V_K)) & if \quad V_{ds} > V_K \\ 0 & if \quad V_{ds} \leq V_K \end{cases}$$

The quantities C_1, C_2, V_K are fitting parameters and $\mathrm{expint}(x) = \int_x^\infty \frac{e^{-t}}{t} dt$. For the practical range of x values this function is well approximated by a few terms in the asymptotic approximation $\mathrm{expint}(x) = e^{-x} [\frac{1}{x} - \frac{1}{x^2} + .. + (-1)^j \frac{j!}{x^{j+1}} + ..]$. Analytical equations are preferred in SPICE for computational speed.

4 Results

The model works well for both long and short channel devices in a half micrometer SOS technology. Figures 1 and 2 show complete sets of characteristics for devices with L = 12 and W = 12 and L = 0.5, W = 1.2. The units of length and width are in micrometer, and the gate voltage is in units of volt. The mathematics permits fairly accurate fitting to measured data. The model will be tested in the future for much smaller channel lengths when the technology is available thru the MOSIS service. However, we strongly believe there are enough applications to a half micrometer SOS technology that the model could bring benefit. Some additional work will be required to install this model into a SPICE simulation tool for further experimental verification of accuracy. But we believe the SPICE speed of convergence will not be an issue because a non-convergence in

SPICE computation usually occurs when there is a discontinuity in the model and our model doesn't show any bad behavior on the output conductance, derivatives of the current.

5 Acknowledgments

6 References

[1]   E J-P Collinge, Silicon-on-Insulator Technology:Materials to VLSI, 2nd Ed.,Kluwer 1997.

[2]   J. Kuo, K-W. Su, *"CMOS VLSI Engineering Silicon-on-Insulator (SOI),"* Kluwer 1998.

[3]   S R. Banna, P. C. H. Chan, M. Chan, and P. K. Ko, "A physically based device model for fully depleted SOI mosfet," IEDM 95,   pp. 949-952, 1995.

[4]   T. C. Hsiao, N. A. Kistler, and J. C. Woo, "Modeling the I-V characteristics of fully depleted submicrometer SOI MOSFET's", IEEE Electron Device Letters, Vol 15, No. 2, pp. 45-47,1994.

[5]   S-J. Jang, B-R Huang, and J-J Ju, "A unified fully depleted and partially depleted SOI MOSFET model", IEEE Transactions on Electron Devices, Vol 46, No. 9, pp. 1872-1876, 1999.

[6]   M. J. Ward, F. M. Odeh, and D. S. Cohen, "Asymptotic methods for metal oxide semiconductor field effect transistor," SIAM. J.Appl.Math, Vol.50, No.4, pp. 1099-1125, August 1990.

[7]   M. J. Ward ,"Singular Perturbations and a Free Boundary Problem in the Modeling of Field-Effect Transistors," SIAM J.Appl.Math Vol. 52, No. 1, pp. 112-139, February 1992.

[8]   S. Sze, *"Physics of semiconductor devices,"* John Wiley, New York, 1969.

[9]   Y. Tsvidis, *"Operation and Modeling of the MOS Transistor,"* McGraw-Hill Book Company, 1987

[10] J. Kervorkian, J. D. Cole, *"Multiple Scale and Singular Perturbation Methods, Applied Mathematical Sciences"*, Vol.114, Springer-Verlag, May 1996.

[11] S Please, C., "An analysis of semiconductor P-N junctions," IMA J. Appl. Math. 28, pp. 301-318, 1982.

[12] Cumberbatch, H. Abebe and H. Morris, "Current-Voltage characteristics from an asymptotic analysis of the MOSFET equations," Journal of Engineering Mathematics, Vol. 19, 1, pp.25-46, 2001.

[13] H. C. de Graaff and F. M. Klaassen, *"Compact Transistor Modelling for Circuit Design,"* Springer-Verlag, 1990.

[14] M. D. Jacunski, M. S. Shur, A. A. Owusu, T. Ytterdal, M. Hack and B. Iniguez, "A short channel DC SPICE model for polysilicon thin-film transistors including temperature effects", IEEE Transactions on Electron Devices, 46, pp1146-1157, 1999.

[15] Z. Yu, R. W. Dutton, and R. A. Kiehl, "Circuit/Device modeling at the quantum level," *IEEE, Computational Electronics, Sixth International Workshop*, pp. 222-229, July 1998.

TABLES

Table 1.Primary Notation and Symbols

Symbol	Quantity
x_1, x_2	coordinates and perpendicular to the channel
L, W	channel length and width
N	doping profile
E, ψ	electric Field and potential
φ_n	quasi Fermi potential for electrons
μ	typical electron mobility magnitude
ε_s	dielectric constant of the semiconductor
ε_i	dielectric constant of the insulator
n_i	intrinsic carrier concentration
q	charge of a proton
k	Boltzmann's constant
T	lattice Temperature assumed constant
$V_{th} = kT / q$	thermal voltage
$L_D = kT\varepsilon_s / n_i q^2$	Debye length
V_{ds}	drain-to-source voltage
V_{gs}	gate-to-source voltage
V_{fb}	flat-band voltage
I_{ds}	source-to-drain current

Table 2.Scaled Variables

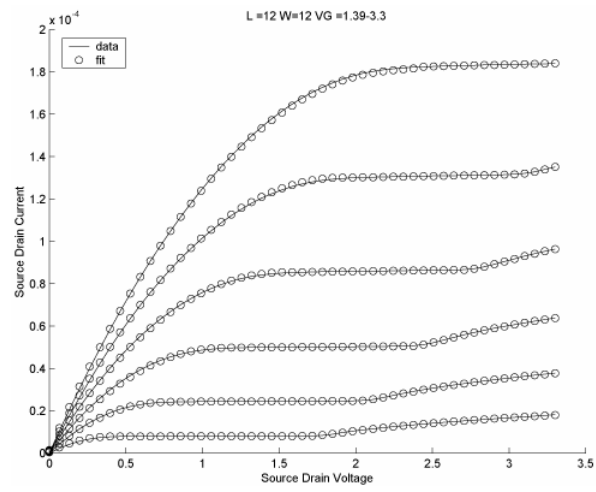| |
|---|
| $\lambda = \max(N(x_1) / n_i)$ |
| $x_1 = L_D \dfrac{\ln(\lambda)}{\lambda} x, \; x_2 = Ly$ |
| $d(x) = N(L_D \dfrac{\ln(\lambda)}{\lambda} x) n_i^{-1}$ |
| $(\psi, \varphi_n) = V_{th}(w, \varphi)$ |
| $V_{gs} - V_{fb} = V_{th}(\bar{V}_{gs} - \ln(\lambda)) = V_{th}\ln(\lambda)V_{gs}^*$ |
| $V_{ds} = V_{th}\bar{V}_{ds}$ |

FIGURES

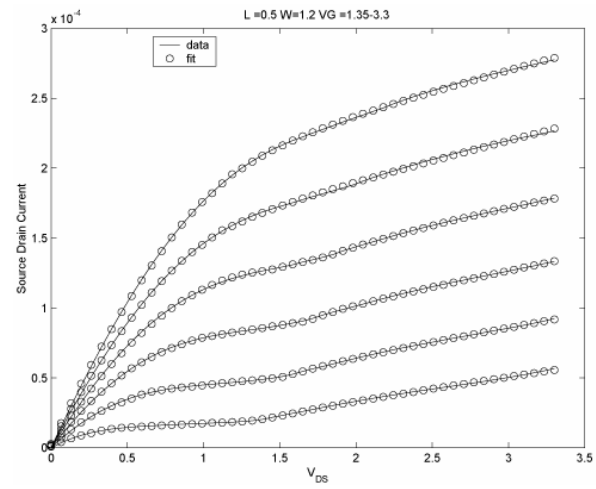Figure 1.The I-V characteristics of a long channel device.

Figure 2.The I-V characteristics of a short channel device.